PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10074732	02/13/2002	257	250	~~2815~~ 2811	Eddie Lee

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**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiners's initials

ATTORNEY DOCKET NO
SC11805TP

TITLE : Method of forming a vertical double gate semiconductor device and structure thereof

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims; Print Claim for O.G
ISSUE FEE: Amount Due; Date Paid	Primary Examiner	DRAWING: Sheets Drwg.; Figs.Drwg.; Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner

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